AMENDMENTS TO THE CLAIMS

1-39. Cancelled.

40. (Currently amended) A communication device for W-CDMA signal transmission and reception, which is software configurable, comprising:

a W-CDMA transmitter comprising at least one of a RAM and registers;

a W-CDMA receiver comprising at least one of a RAM and registers;

a signal acquisition circuit

a digital circuit for phase unbalance precompensation ~~comprised~~ in said W-CDMA transmitter, wherein said digital circuit ~~comprising:~~

~~an input register holding a compensation angle; and~~

~~section adapted to perform arithmetic calculations to acquire a change of an I, Q angle by the compensation angle~~ substantially removes the I, Q phase difference that causes the phases of I and Q signals to not have a 90 degree separation.

41. (Previously presented) The communication device of Claim 40, further comprising a circuit for noise and interference estimation, said circuit comprising:

means to acquire a programmable number of absolute value accumulations at a chip rate or an oversampled chip rate; and

a programmable low pass filter to average the noise and interference estimations.

42. (Previously presented) The communication device of Claim 40, further comprising a circuit for initial synchronization, said circuit comprising:

a matched filter, energy calculation and accumulating RAM for slot synchronization;

a set of correlators for frame synchronization and code group identification;

an energy estimation block; and

maximum detection means readable by a microprocessor subsystem.

43. (Previously presented) The communication device of Claim 40, further comprising circuitry to generate packet data transmission, said circuitry comprising:

a buffer storing data and activity bits;

I, Q spreaders and gain control means;

scrambling code generator and scrambling means; and

means for packet timing through RX frame edge triggering.

44. (Previously presented) The communication device of Claim 43, wherein the communication device is configured for RACH transmission in UMTS/FDD.

45. (Previously presented) The communication device of Claim 40, further comprising a processor.

46. (Previously presented) The communication device of Claim 45, wherein the processor is configured to reconfigure the communication device.

47. (Previously presented) The communication device of Claim 45, wherein the processor controls at least one of the RAM registers of said W-CDMA signal transmitter and receiver.

48. (Previously presented) The communication device of Claim 45, wherein the transmitter comprises a first programmable pulse shaping filter, and wherein the receiver comprises a second programmable pulse shaping filter.

49. (Previously presented) The communication device of Claim 48, wherein the pulse shaping filters are programmable to perform GMSK filtering, and wherein said transmitter and receiver are arranged to interface with a GSM front-end.

50. (Previously presented) The communication device of Claim 49, wherein the processor performs a GSM protocol stack.

51. (Previously presented) The communication device of Claim 42, wherein the communication device is configured for at least one of waveform transmission, reception and acquisition of signals selected from the group consisting of UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB signals.

52. (Previously presented) The communication device of Claim 40, wherein said transmitter comprises one or more elements selected from the group consisting of:

synchronization hardware to slave transmit start epochs to events external to the transmitter;

a burst generator for realizing discontinuous transmissions;

a QPN channel containing one or more spreaders with their own amplification of the output;

a combiner to accumulate the QPN channel output;

a PN code generator;

a scrambling code generator;

a scrambler;

a combiner which accumulates the scrambling code output;

a pulse shaping oversampling filter; and

an NCO and upconverter for carrier precompensation.

53. (Previously presented) The communication device of Claim 52, wherein the PN code generator is realized as a RAM in which PN codes are downloaded under control of the processor.

54. (Previously presented) The communication device of Claim 52, wherein the scrambling code generator is realized as a programmable Gold Code generator.

55. (Previously presented) The communication device of Claim 52, wherein the QPN channel is arranged to execute UMTS forward or return link transmission.

56. (Previously presented) The communication device of Claim 52, wherein an amplification of the spreader output is arranged to perform transmit power control.

57. (Previously presented) The communication device of Claim 40, wherein the transmitter comprises a time interpolator to perform sub-chip time alignments.

58. (Previously presented) The communication device of Claim 40, wherein the transmitter is arranged for multi-code transmission.

59. (Previously presented) The communication device of Claim 40, wherein the receiver comprises:

a pulse shaping filter;

an optional level control block;

a demodulator assigned to track multi-path components received from one base station; and

a reference demodulator for S/ (N+I) measurements.

60. (Previously presented) The communication device of Claim 59, wherein said receiver further comprises a downconverter prior to said pulse shaping filter in order to interface at a front-end at an intermediate frequency.

61. (Previously presented) The communication device of Claim 59, wherein the receiver is arranged for execution of at least one of UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB forward link and return link waveforms.

62. (Previously presented) The communication device of Claim 59, wherein the level control block comprises:

a programmable shifter to perform coarse grain dynamic control;

a programmable multiplier to perform fine grain dynamic control;

an overflow counter operating on a most significant bit and a second most significant bit; and

a saturation logic to clip a result from the multiplier.

63. (Previously presented) The communication device of Claim 59, wherein the level control block is operated in a runtime control loop by the processor.

64. (Previously presented) The communication device of Claim 59, wherein the demodulator comprises:

a Rake filter producing a signal at a chip rate which is a coherent accumulation of channel corrected multipath components resulting from one base station;

a tracking unit using said signal at the chip rate for descrambling and despreading a plurality of waveform channels; in which said Rake filter comprises:

a FIFO to buffer samples at chip rate coming from said level control block;

a delay line containing a plurality of registers, an input of the delay line being connected to an output of said FIFO;

a plurality of finger blocks, inputs of said finger blocks being connected to programmable tap positions on said delay line; and

a summator of complex outputs of said finger blocks at chip rate.

65. (Previously presented) The communication device of Claim 64, wherein the finger blocks are respectively grouped in a late multipath group and an early multipath group, the Rake filter being arranged to accumulate the energies of the outputs of said late multipath group and said early multipath group, and to use these accumulated values to feed the time error detector of the DLL for time tracking.

66. (Previously presented) The communication device of Claim 64, wherein the Rake filter comprises memories to hold at least one of a spreading code for a channel correction Pilot, a scrambling code for a channel correction Pilot, a channel correction Pilot symbol modulation, and a channel correction Pilot symbol activities.

67. (Previously presented) The communication device of Claim 66, wherein the memories are controlled by the processor.

68. (Previously presented) The communication device of Claim 66, wherein the finger block comprises:

a channel correction Pilot descrambler;

a channel correction Pilot despreader;

a channel correction Pilot filter, first performing a coherent channel correction Pilot symbol accumulation over a programmable number of steps, and secondly producing a weighted average on a programmable number of said coherent channel correction Pilot symbol accumulation over a programmable number of steps;

a channel estimator generating a channel estimation at chip rate, using outputs of said Pilot filter;

a channel corrector performing a multiplication of an incoming chip stream with a complex conjugate of said channel estimation;

a calculation of a slot energy;

a comparison of the slot energy with a programmable threshold; and

a circuit to force said channel estimation to zero if said threshold is not exceeded.

69. (Previously presented) The communication device of Claim 68, wherein the finger is arranged for slow and fast fading compensation, by programming the channel correction Pilot filter for slow fading, said channel correction Pilot filter first performing a coherent accumulation over a slot, and secondly performing a weighted average over previous-previous, previous, actual and next obtained slot values, yielding a channel estimation per slot, which is applied by said channel corrector; and for fast fading, said channel correction Pilot filter first performing a coherent accumulation over a slot, and then deriving channel estimations through interpolating consecutive said coherent accumulations over a slot, yielding channel estimations with sub-symbol timing, which are applied by said channel corrector.

70. (Previously presented) The communication device of the Claim 59, wherein the reference demodulator comprises:

an accumulator of programmable length of the absolute values of samples at chip rate; and

a low pass filter operating on said accumulator output.

71. (Previously presented) The communication device of Claim 59, wherein the reference demodulator is arranged to operate in a runtime control loop by the processor.

72. (Previously presented) The communication device of Claim 59, wherein the demodulator is arranged to perform satellite diversity.

73. (Previously presented) The communication device of Claim 40, wherein the communication device is configured to perform accurate ranging measurements to geostationary satellites.

74. (Currently amended) An integrated circuit comprising a communication device for W-CDMA signal transmission and reception, which is software configurable, the communication device comprising:

a W-CDMA transmitter comprising at least one of a RAM and registers;

a W-CDMA receiver comprising at least one of a RAM and registers;

a signal acquisition circuit;

a digital circuit for phase unbalance precompensation ~~comprised~~ in said W-CDMA transmitter, wherein said digital circuit ~~comprising:~~

~~an input register holding a compensation angle; and~~

~~a section adapted to perform arithmetic calculations to acquire a change of an I, Q angle by the compensation angle~~ substantially removes the I, Q phase difference that causes the phases of I and Q signals to not have a 90 degree separation.

75. (Currently amended) A method of operating a W-CDMA communication device comprising a W-CDMA transmitter comprising at least one of a RAM and registers, a W-CDMA receiver comprising at least one of a RAM and registers, a signal acquisition circuit, a digital circuit for phase unbalance precompensation ~~comprised~~ in said W-CDMA transmitter, wherein said digital circuit ~~comprises an input register holding a compensation angle and a section adapted to perform arithmetic calculations to acquire a change of an I, Q angle by the~~

~~compensation angle~~ substantially removes the I, Q phase difference that causes the phases of I and Q signals to not have a 90 degree separation, the method comprising:

configuring said device for a specific use, and

performing at least one of transmitting, receiving and acquiring waveform signals.

76. (Previously presented) The method of Claim 75, wherein said waveform signals are selected from the group consisting of UMTS, Satellite UMTS, Galileo, GPS, IS-2000, IMT-2000, CDMA2000, IS-95, 3GPP, 3GPP2 and ARIB signals.

77. (Previously presented) The method of Claim 75, wherein said configuring is done by a processor.

78. (Previously presented) A communication device for W-CDMA signal transmission and reception, which is software configurable, comprising:

a W-CDMA transmitter comprising at least one of a RAM and registers;

a W-CDMA receiver comprising at least one of a RAM and registers;

a signal acquisition circuit;

a digital circuit for phase unbalance precompensation comprised in said W-CDMA transmitter, said digital circuit comprising:

an input register holding a compensation angle; and

a section adapted to perform arithmetic calculations to acquire a change of an I, Q angle by the compensation angle;

wherein the W-CDMA receiver comprises a level block control, the level block control comprising:

a programmable shifter to perform coarse grain dynamic control;

a programmable multiplier to perform fine grain dynamic control;

an overflow counter operating on a most significant bit and a second most significant bit; and

a saturation logic to clip a result from the multiplier.

79. (Previously presented) A communication device for W-CDMA signal transmission and reception, which is software configurable, comprising:

a W-CDMA transmitter comprising at least one of a RAM and registers;

a W-CDMA receiver comprising at least one of a RAM and registers;

a signal acquisition circuit;

a digital circuit for phase unbalance precompensation comprised in said W-CDMA transmitter, said digital circuit comprising:

an input register holding a compensation angle; and

a section adapted to perform arithmetic calculations to acquire a change of an I, Q angle by the compensation angle;

wherein the W-CDMA receiver comprises a demodulator assigned to track multi-path components received from one base station, wherein the demodulator comprises:

a Rake filter producing a signal at a chip rate which is a coherent accumulation of channel corrected multipath components resulting from one base station;

a tracking unit using said signal at the chip rate for descrambling and despreading a plurality of waveform channels; in which said Rake filter comprises:

a FIFO to buffer samples at chip rate coming from said level control block;

a delay line containing a plurality of registers, an input of the delay line being connected to an output of said FIFO;

a plurality of finger blocks, inputs of said finger blocks being connected to programmable tap positions on said delay line; and

a summator of complex outputs of said finger blocks at chip rate.

80. (Previously presented) The communication device of Claim 79, wherein the finger blocks are respectively grouped in a late multipath group and an early multipath group, the Rake filter being arranged to accumulate the energies of the outputs of said late multipath group and said early multipath group, and to use these accumulated values to feed the time error detector of the DLL for time tracking.

81. (Previously presented) The communication device of Claim 79, wherein the Rake filter comprises memories to hold at least one of a spreading code for a channel

correction Pilot, a scrambling code for a channel correction Pilot, a channel correction Pilot symbol modulation, and a channel correction Pilot symbol activities.

82. (Previously presented) The communication device of Claim 81, wherein the memories are controlled by the processor.

83. (Previously presented) The communication device of Claim 81, wherein the finger block comprises:

a channel correction Pilot descrambler;

a channel correction Pilot despreader;

a channel correction Pilot filter, first performing a coherent channel correction Pilot symbol accumulation over a programmable number of steps, and secondly producing a weighted average on a programmable number of said coherent channel correction Pilot symbol accumulation over a programmable number of steps;

a channel estimator generating a channel estimation at chip rate, using outputs of said Pilot filter;

a channel corrector performing a multiplication of an incoming chip stream with a complex conjugate of said channel estimation;

a calculation of a slot energy;

a comparison of the slot energy with a programmable threshold; and

a circuit to force said channel estimation to zero if said threshold is not exceeded.

84. (Previously presented) The communication device of Claim 83, wherein the finger is arranged for slow and fast fading compensation, by programming the channel correction Pilot filter for slow fading, said channel correction Pilot filter first performing a coherent accumulation over a slot, and secondly performing a weighted average over previous-previous, previous, actual and next obtained slot values, yielding a channel estimation per slot, which is applied by said channel corrector; and for fast fading, said channel correction Pilot filter first performing a coherent accumulation over a slot, and then deriving channel estimations through interpolating consecutive said coherent accumulations over a slot, yielding channel estimations with sub-symbol timing, which are applied by said channel corrector.

85. (New) The communication device of Claim 40, wherein the digital circuit performs arithmetic calculations to substantially remove the I, Q phase difference, the calculations comprising:

$I_{out} + I_{in} + Q_{in} * \tan(ß)$, and

$Q_{out} + Q_{in} + I_{in} * \tan(ß)$,

where a compensation angle is 2ß.

86. (New) The communication device of Claim 40, wherein the digital circuit uses a software configurable compensation angle.

87. (New) The communication device of Claim 40, wherein the digital circuit comprises:

an input register holding a compensation angle; and

a section adapted to perform arithmetic calculations to acquire a change of the I, Q angle by the compensation angle.

88. (New) The integrated circuit of Claim 74, wherein the digital circuit performs arithmetic calculations to substantially remove the I, Q phase difference, the calculations comprising:

$I_{out} + I_{in} + Q_{in} * \tan(ß)$, and

$Q_{out} + Q_{in} + I_{in} * \tan(ß)$,

where a compensation angle is 2ß.

89. (New) The integrated circuit of Claim 74, wherein the digital circuit uses a software configurable compensation angle.

90. (New) The integrated circuit of Claim 74, wherein the digital circuit comprises:

an input register holding a compensation angle; and

a section adapted to perform arithmetic calculations to acquire a change of the I, Q angle by the compensation angle.

91. (New) The method of Claim 75, wherein the digital circuit performs arithmetic calculations to substantially remove the I, Q phase difference, the calculations comprising:

$I_{out} + I_{in} + Q_{in} * \tan(\text{ß})$, and

$Q_{out} + Q_{in} + I_{in} * \tan(\text{ß})$,

where a compensation angle is 2ß.

92. (New) The method of Claim 75, wherein the digital circuit uses a software configurable compensation angle.

93. (New) The method of Claim 75, wherein the digital circuit comprises:

an input register holding a compensation angle; and

a section adapted to perform arithmetic calculations to acquire a change of the I, Q angle by the compensation angle.